

Digital Window Watchdog Timer

Description

The digital window watchdog timer, U5021M, is a CMOS integrated circuit. In application where safety is critical, it is especially important to monitor the microcontroller. Normal microcontroller operation is indicated by a cyclically transmitted trigger signal, which is received by a window watchdog timer within a defined time window. A missing or a wrong trigger signal makes the watchdog

timer reset the microcontroller. The IC is tailored for microcontrollers which can work in both full-power and sleep mode. With an additional voltage monitoring (power-on reset and supply voltage drop reset) U5021M offers a complete monitoring solution for microsystems in automotive and industrial applications.

Features

- Low current consumption: $I_{DD} < 100 \mu A$
- RC-oscillator
- Internal reset during power up and supply voltage drops (POR)
- “Short” trigger window for active mode
“long” trigger window for sleep mode
- Cyclical wake-up of micro in sleep mode
- Trigger input
- Single wake-up input
- Reset output
- Enable output

Case: SO8

Block Diagram

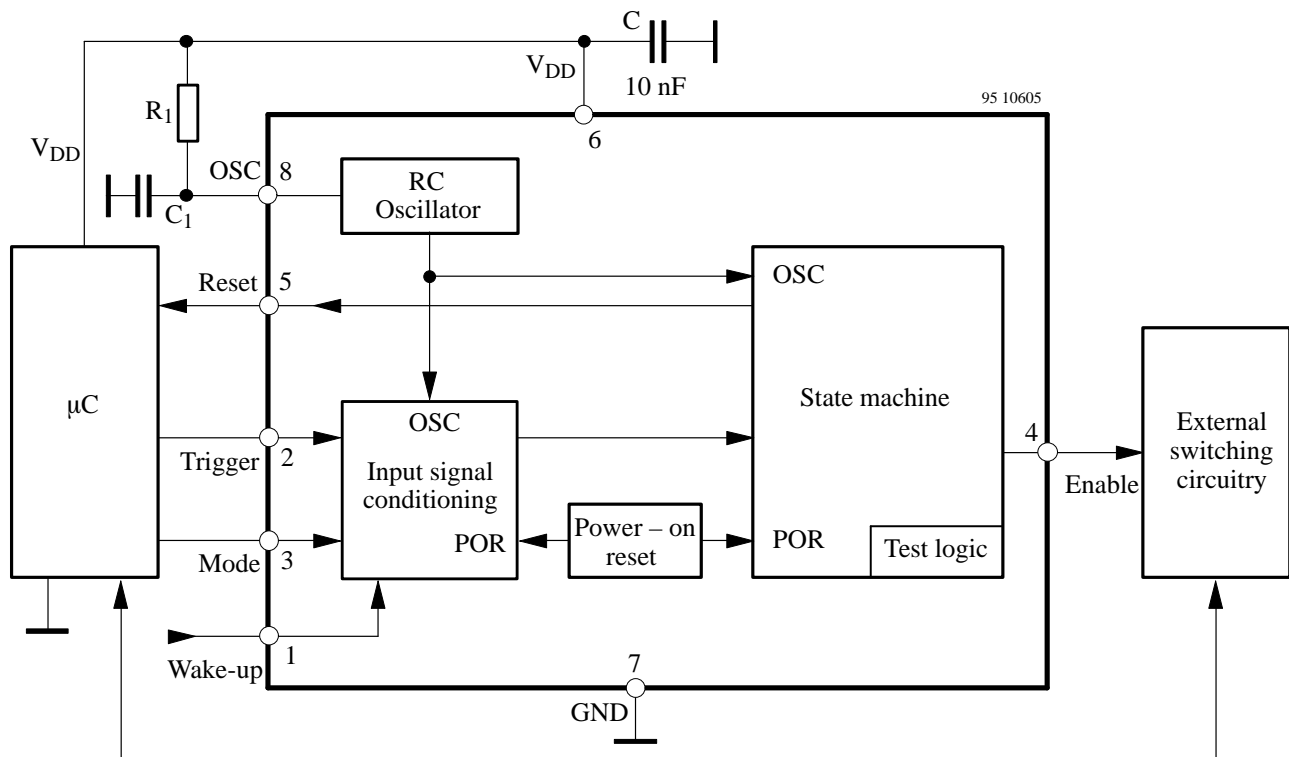


Figure 1. Block diagram with external circuit

Pin Description

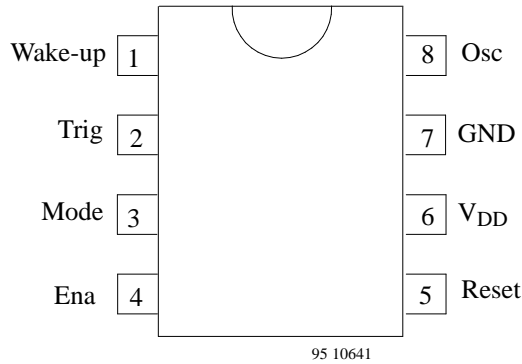


Figure 2.

Pin	Symbol	Function
1	Wake-up	There is one digitally debounced wake-up input. During the long trigger mode each signal slope at the input initiates a reset pulse at Pin 5.
2	Trig	Trigger input It is connected to the microprocessor's trigger signal.
3	Mode	Mode input The processor's mode signal initiates the switchover between the long and the short watchdog time.
4	Ena	Enable output It is used for the control of peripheral components. It is activated after the processor triggers three times correctly.
5	Reset	Reset output Resets the processor in the case of a trigger error or if a wake-up pulse occurs during the long watchdog period.
6	V _{DD}	Supply voltage
7	GND	Ground, reference voltage
8	Osc	RC oscillator

Functional Description

Supply, Pin 6

The U5021M requires a stabilized supply voltage $V_{DD} = 5\text{ V} \pm 5\%$ to comply with its electrical characteristic.

An external buffer capacitor of $C = 10\text{ nF}$ may be connected between Pin 6 and GND.

RC-Oscillator, Pin 8

The clock frequency, f , can be adjusted with the components R_1 and C_1 according to the formula:

$$f = \frac{1}{t}$$

where $t = 1.35 + 1.57 R_1 (C_1 + 0.01)$

R_1 in $k\Omega$, C_1 in nF and t in μs

The clock frequency determines all time periods of the logic part as shown in the last section of the data sheet (timing). With an appropriate selection of components, the clock frequency, f , is nearly independent of the supply voltage as shown in figure 3. Frequency tolerance $\Delta f_{\max} = 10\%$ with $R_1 \pm 1\%$, $C_1 = \pm 5\%$.

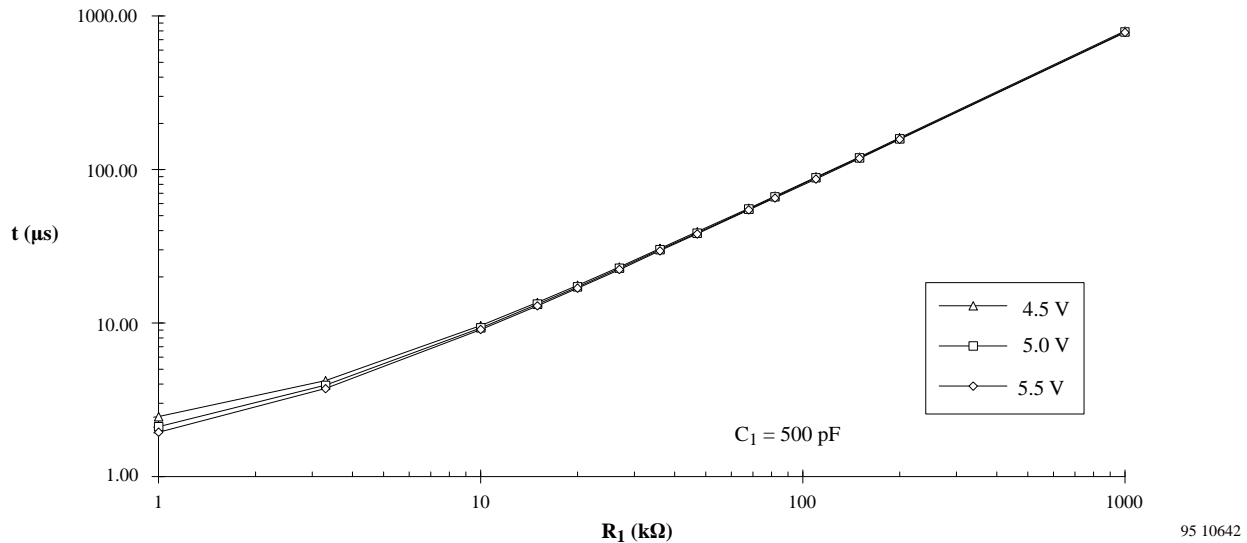


Figure 3. Period t vs. R_1 , @ $C_1 = 500$ pF

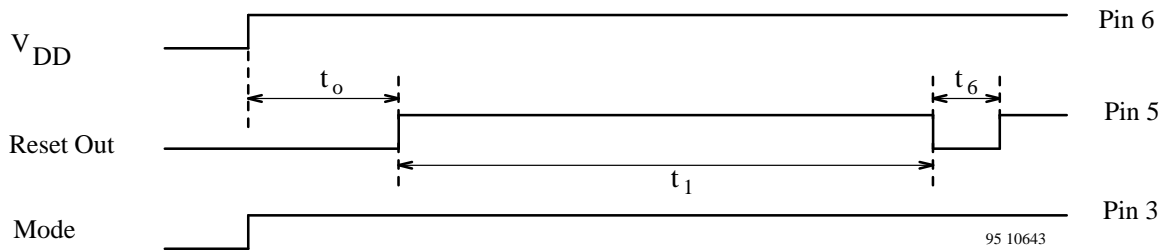


Figure 4. Power-up reset and mode switchover

Supply Voltage Monitoring, Pin 5

The integrated power-on reset (POR) circuitry sets the internal logic to a defined basic status and generates a reset pulse at the reset output, Pin 5, during ramp-up of the supply voltage and in the case of voltage drops of the supply. A hysteresis in the POR threshold prevents the circuit from oscillating. During ramp-up of the supply voltage the reset output stays active for time, t_o , in order to bring the microcontroller in its defined reset status (see figure 4).

Switchover Mode Time, Pin 3

The switchover mode time enables the synchronous operation of micro and watchdog. After the power-up reset time the watchdog has to be switched to its monitoring mode by the micro with a “low” signal transmitted to the mode pin (Pin 3) within the time out period, t_1 . If the low signal does not occur within time, t_1 , (see figure 4) the watchdog generates a reset pulse, t_6 , and the

time, t_1 , starts again. Micro and watchdog are synchronized with the switchover mode time, t_1 , each time a reset pulse is generated.

Microcontroller in Active Mode

Monitoring with the “Short” Trigger Window

After the switchover mode the watchdog works in the short watchdog mode and expects a trigger pulse from the micro within the defined time window, t_3 , (enable time). The watchdog generates a reset pulse which resets the micro if

- the trigger pulse duration is too long,
- the trigger pulse is within the disable time, t_2
- there is no trigger pulse

Figure 5 shows the pulse diagram with a missing trigger pulse.

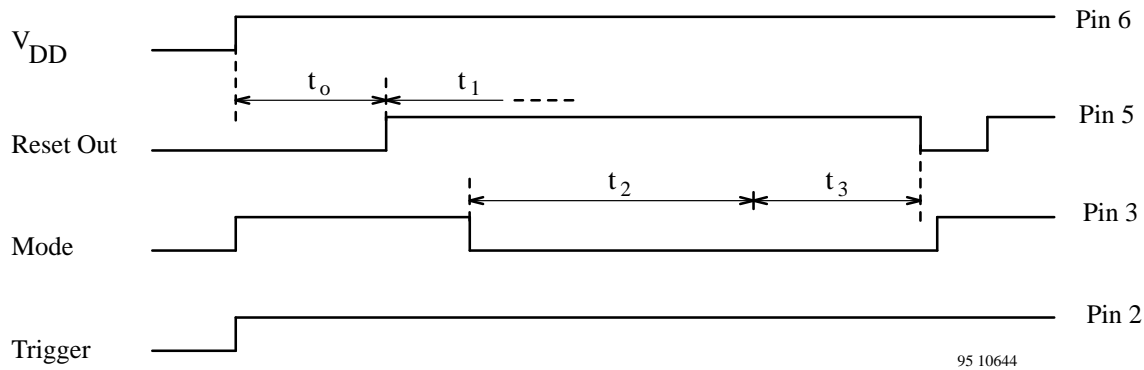
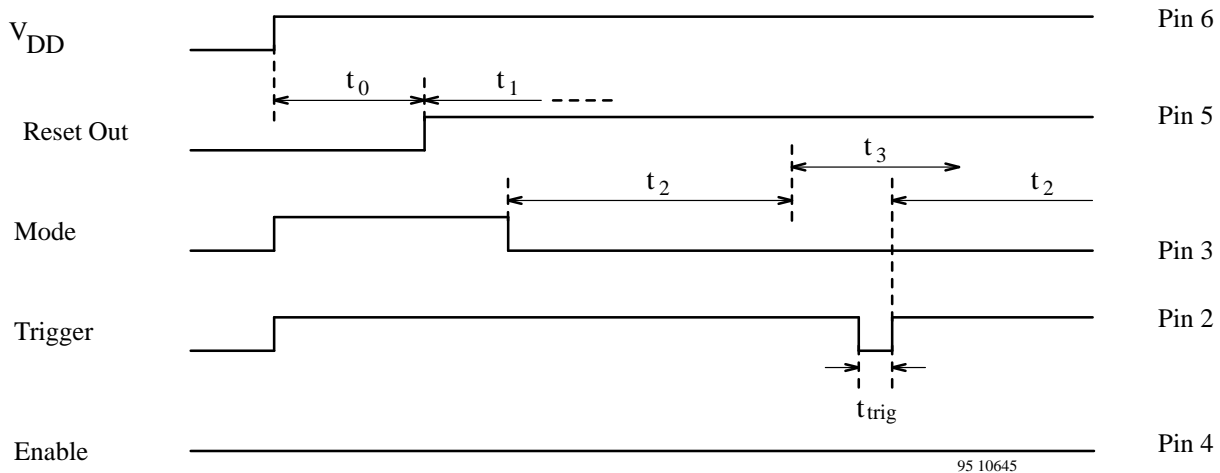


Figure 5. Pulse diagram with no trigger pulse during the short watchdog time

Figure 6 shows a correct trigger sequence. The positive edge of the trigger signal starts a new monitoring cycle with the disable time, t_2 . To ensure a correct operation of the micro the watchdog needs to be triggered three times correctly before it sets its enable output. This feature is used to activate or deactivate safety critical components,

which have to be switched to a certain condition (emergency status) in the case of a micro malfunction. As soon as there is an incorrect trigger sequence the enable signal is reset and it takes again a three correct trigger sequence before enable is reset.

Figure 6. Pulse diagram of a correct trigger sequence during the short watchdog time



Microcontroller in Sleep Mode Monitoring with the “Long” Trigger Window

The long watchdog mode allows cyclical wake up of the micro during the sleep mode. Like in the short watchdog mode there is a disable time, t_4 , and an enable time, t_5 , in which a trigger signal is accepted. The watchdog can be switched from the short trigger window to the long trigger window with a “high” potential at the mode pin (Pin 3). In contrast to the short watchdog mode the time periods

are now much longer and the enable output remains inactive that other components can be switched off to effect a further decrease in current consumption. As soon as a wake-up signal at the wake up input (Pins 1) is detected, the long watchdog mode ends, a reset pulse wakes-up the sleeping micro and the normal monitoring cycle starts with the mode switchover time.

Figure 7 shows the switchover from the short to the long watchdog mode. The wake up signal during the enable time, t_5 , activates a reset pulse, t_6 .

The watchdog can be switched back from the long to the short watchdog mode with a low potential at the mode pin (Pin 3).

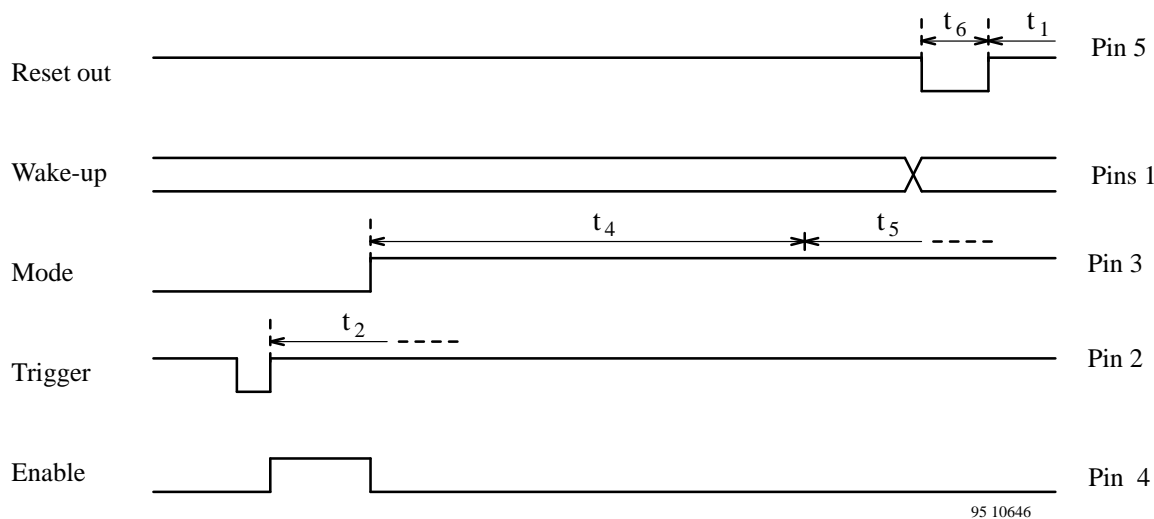


Figure 7. Pulse diagram of the long watchdog time

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_{DD}	6.5	V
Output current	I_{OUT}	± 2	mA
Input voltage	V_{IN}	-0.5 V to $V_{DD} + 0.5$ V	
Ambient temperature range	T_{amb}	-40 to +125	°C
Storage temperature range	T_{stg}	-55 to +150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SO8	R_{thJA}	180	K/W

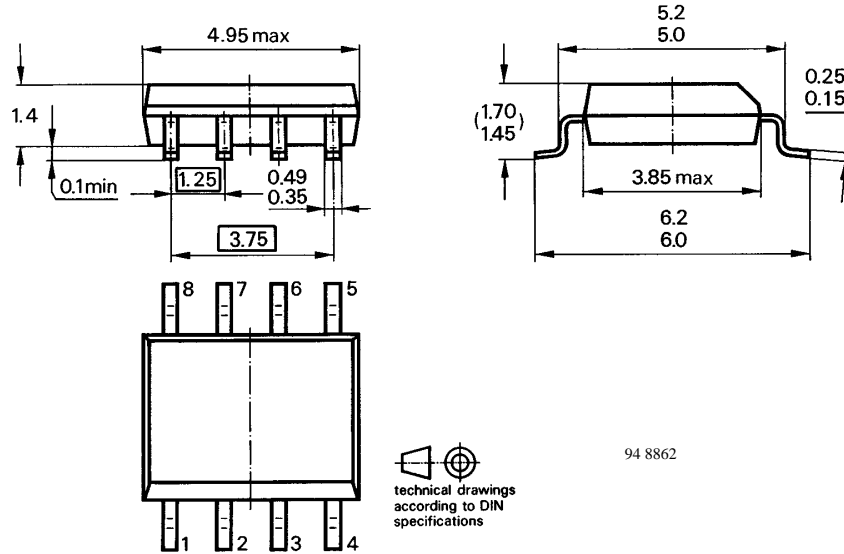
Electrical Characteristics

$V_{DD} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; reference point is ground (Pin 7); figure 4, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 6	V_{DD}	4.5		5.5	V
Current consumption	$R_I = 66\text{ k}\Omega$ Pin 6	I_{DD}			100	μA
Power-on reset	Logic functions Pin 6	V_{DD}	1			V
Power-on reset	Threshold Pin 6	V_{POR}		3.8		V
Power-on reset	Hysteresis Pin 6	V_{hys}		100		mV
Inputs Pins 1, 2, and 3						
Upper threshold ("1")		V_{IH}	4.0			V
Lower threshold ("0")		V_{IL}			1.0	V
Input voltage range		V_{IN}	-0.4		V_{DD}	V
Input current		I_{IN}			1	μA
Outputs Pins 4 and 5						
Max. output current		I_{OUT}	2			mA
Upper output voltage ("1")	$I_{OUT} = 1\text{ mA}$	V_{OH}	4.2			V
Lower output voltage ("0")	$I_{OUT} = -1\text{ mA}$	V_{OL}			0.8	V
Timing						
Debounce period	Trig, Mode, Pins 2 and 3		3		4	cyc
Debounce period	Wake-up, Pin 1		96		128	cyc
Max. trigger pulse period				45		cyc
Power-up reset time		t_0		201		cyc
Time out period		t_1		1112		cyc
Enable time	Short	t_3		124		cyc
	Long	t_5		30002		cyc
Disable time	Short	t_2		130		cyc
	Long	t_4		71970		cyc
Reset out time		t_6		40		cyc

Dimensions in mm

Package. SO8



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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